ADSANTEC
Ultra High-Speed Mixed Signal ASICs

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ASNT_PRBS43A
40Gbps 2^7-1 PRBS Generator with USB Control Interface

- 14ps Rise/Fall time for muxed PRBS data output
- 17ps Rise/Fall time for sync output
- 19ps Rise/Fall time for half-rate data outputs
- VCO frequencies from 7.4*GHz* to 32.1*GHz*
- User selectable clock divide by 2 to 512 sync output for scope triggering
- GUI software interface with onboard USB

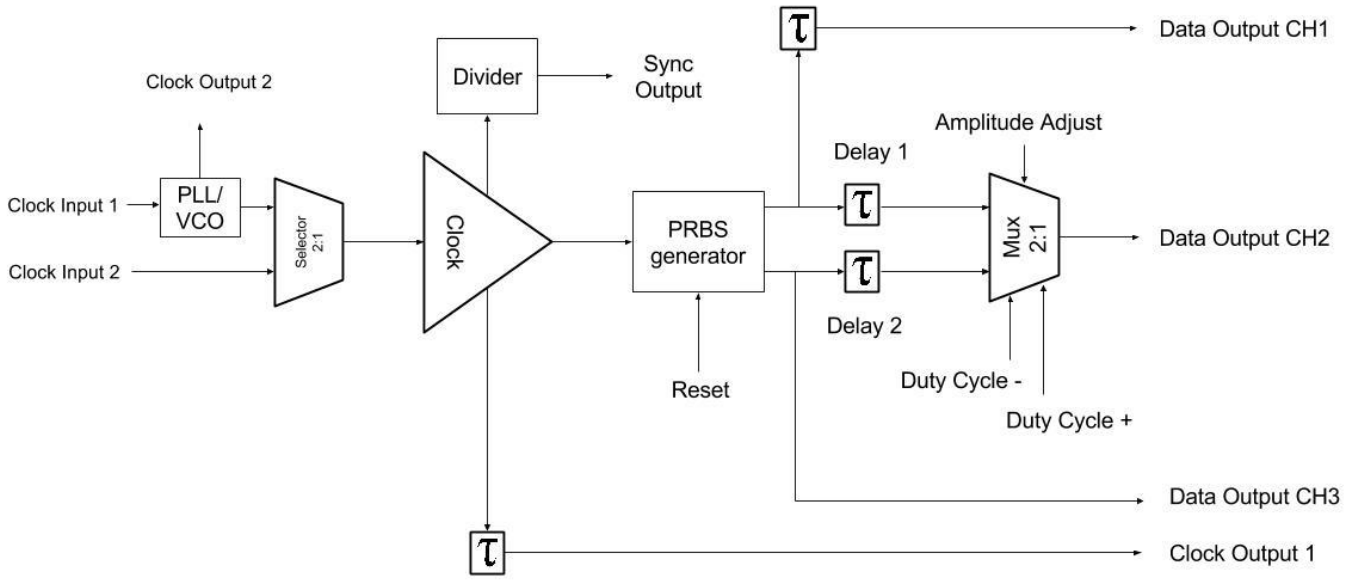

Figure 1. Block Diagram

DESCRIPTION

The ASNT_PRBS43A can be used for test applications, design verification, and R&D environments. The 2^7-1 pseudo random bit sequence (PRBS) generator operates from 10*kbps* to 40*Gbps*. Either an external half-rate clock, or a reference clock to the onboard PLL is needed to generate the required data. Some output clock and data channels have adjustable phase and amplitude. The Sync output provides an oscilloscope triggering signal to view the data pattern or

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eye diagram of PRBS7. A Windows GUI (compatible with Windows XP, 7, 8) is used to control the amplitude, phase, PRBS reset, divide ratio for sync, and clock input control through a USB-B connector on the ASNT_PRBS43A. Power is supplied with an included AC-DC power supply. All data and clock connections shown in **Figure 1** and **Figure 2** are SMA female connectors.

The front panel of the instrument is shown in **Figure 2.** It contains 3 differential data outputs, 1 differential clock output, and a single-ended Sync output.

Figure 2. Front Panel

The back panel of the instrument is shown in **Figure 3.** It contains 1 external single-ended clock input, 1 single-ended clock output, and a single-ended reference clock input. It also includes a power ON/OFF switch, and a +5V DC power supply (included) which connects to a male barrel jack shown in **Figure 3**. The USB-B connector allows connection to a computer for controlling the instrument through a windows GUI.

Figure 3. Back Panel

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Data Outputs

There are 3 differential AC coupled data outputs:

Data Output CH1 has PRBS7 up to 20*Gbps* with a controllable 155*ps* of delay, amplitude control from 0*V* to 1.6*V* differentially, and output duty cycle control from 40% to 60%.

Data Output CH2 has PRBS7 up to 40*Gbps* with amplitude control from 0*V* to 1.6*V* differentially.

Data Output CH3 has PRBS7 up to 20*Gbps* with output amplitude of 0.8*V* differentially.

Clock I/O's

There are 2 single-ended AC coupled clock inputs:

Clock Input 1 (Ref Clk In) is a reference clock input that needs at least 50*mV* of input amplitude to drive the onboard PLL's. The reference frequency range can be found in **Table 1**.

Clock Input 2 (Ext Clk In) is a half-rate clock input that may alternatively be used instead of Clock Input 1 to provide any data rate from 1*Mbps* to 40*Gbps* by providing at least 50*mV* of input amplitude from 1*MHz* to 20*GHz*.

There are 2 AC coupled clock outputs:

Clock Output 1 (front panel) is a differential output ranging from 1*MHz* to 20*GHz* with an adjustable delay up to 105*ps*, and amplitude of 0.8*V peak to peak* differentially.

Clock Output 2 (back panel) is a single-ended output ranging from 24.2*GHz* to 32.1*GHz* with output amplitude of ~0.3*V peak to peak*.

Sync Output

Sync Output provides a selectable clock divided by 2*n with n integer values from 1 to 256 and an AC coupled single-ended output amplitude of 600*mV*. Sync Output can be connected to an oscilloscope's trigger to allow display of a PRBS7 pattern or eye diagram.

Note: All I/O's are AC coupled.

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Table 1. Clock/Data Table

MODE	INPUT				OUTPUT										Unit
	Clock Input 1 (Ref Clk In)		Clock Input 2 (Ext Clk In)		Clock Output 1 (front panel)		Clock Output 2 (back panel)		Data Output CH1		Data Output CH2		Data Output CH3		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
VCO 1	1.5125	2.00625	-	-	12.1	16.05	24.2	32.1	**12.1**	**16.05**	**24.2**	**32.1**	**12.1**	**16.05**	*GHz/**Gbps***
VCO 2	1.5125	2.00625	-	-	6.05	8.025	24.2	32.1	**6.05**	**8.025**	**12.1**	**16.05**	**6.05**	**8.025**	*GHz/**Gbps***
VCO 3	0.61875	0.80625	-	-	9.9	12.9	-	-	**9.9**	**12.9**	**19.8**	**25.8**	**9.9**	**12.9**	*GHz/**Gbps***
VCO 4	0.61875	0.80625	-	-	4.45	6.45	-	-	**4.45**	**6.45**	**9.9**	**12.9**	**4.45**	**6.45**	*GHz/**Gbps***
Ext Clock	-	-	0.001	20	0.001	20	-	-	**0.001**	**20**	**4***	**40**	**0.001**	**20**	*GHz/**Gbps***

Note: 4* - Clock Input must be minimum of 2 *GHz*

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Clock Input 1 (Ref Clk In)					
Single-ended Swing	50	300	600	mV_{PP}	
Frequency	0.0001		20	*GHz*	
Clock Input 2 (Ext Clk In)					
Single-ended Swing	50		1000	mV_{PP}	
Frequency	7.4		32.1	*GHz*	See Table 1.
Clock Output 1 (front panel)					
Differential Swing		1700		mV_{PP}	
Frequency	0.001		20	*GHz*	
Rise/Fall times	13		15	*ps*	
Duty Cycle	45	50	55	*%*	
Delay Adjustment range		105		*ps*	
Clock Output 2 (back panel)					
Single-ended Swing		300 250		mV_{PP}	@ 25GHz @ 27GHz

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		150 200			@ 29GHz @ 32GHz
Frequency	24.2		32.1	*GHz*	
Duty Cycle	45	50	55	*%*	
Data Output CH1					
Differential Swing	0		1700	mV_{PP}	Adjustable
Data Rate	0.001		20	*Gbps*	
Rise/Fall times	6		10	*ps*	20% - 80%
Duty Cycle	45	50	55	*%*	
Delay Adjustment range		165		*ps*	
Absolute delay Stability	-2		2	*ps*	0-125°C
Data Output CH2					
Differential Swing	0		1700	mV_{PP}	Adjustable
Data Rate	4		40	*Gbps*	
Rise/Fall times	6	8	10	*ps*	20% - 80%
Duty Cycle	40		60	*%*	Adjustable
Data Output CH3					
Differential Swing		1200		mV_{PP}	
Data Rate	0.001		20	*Gbps*	
Rise/Fall times	13		15	*ps*	20% - 80%
Duty Cycle	45	50	55	*%*	
Sync Output					
Frequency	0.0001		10	*GHz*	
Single-ended Swing		600		mV_{PP}	
Duty Cycle	47	50	53	*%*	
Rise/Fall time	15	17	19	*ps*	20%-80%
ALL I/O's are AC coupled					

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MECHANICAL DIMENSIONS

PARAMETER	TYP	UNIT	COMMENTS
Length	164	*mm*	
Width	129	*mm*	
Height	58	*mm*	

REVISION HISTORY

Revision	Date	Changes
1.0.1	05-2014	Added figure 2 and 3
1.0.0	03-2014	Preliminary Release